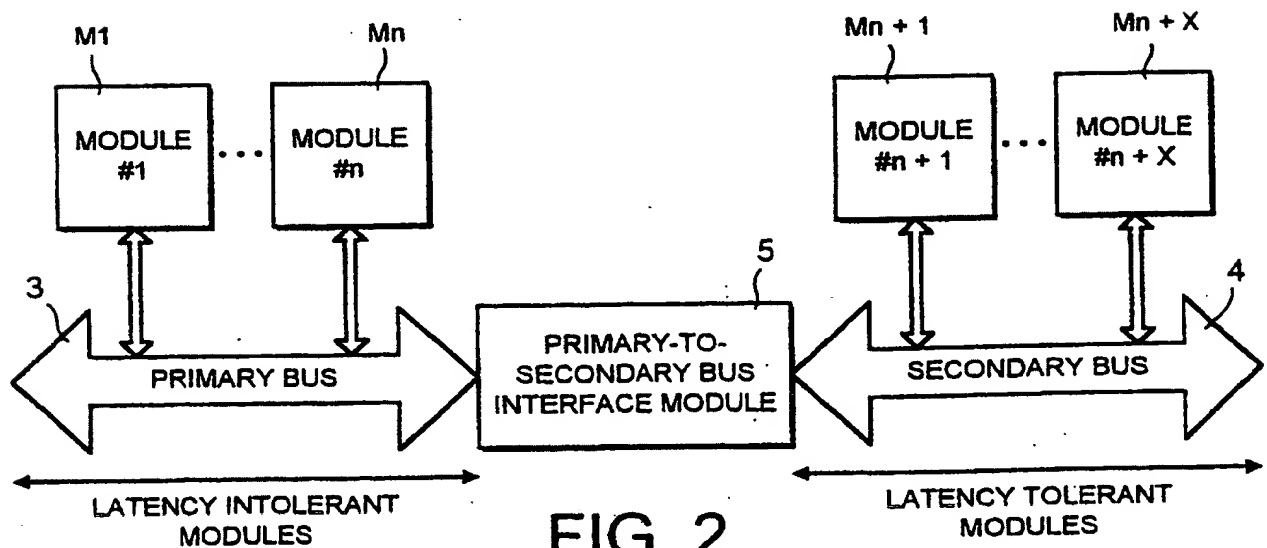


**FIG. 1**  
(PRIOR ART)



**FIG. 2**

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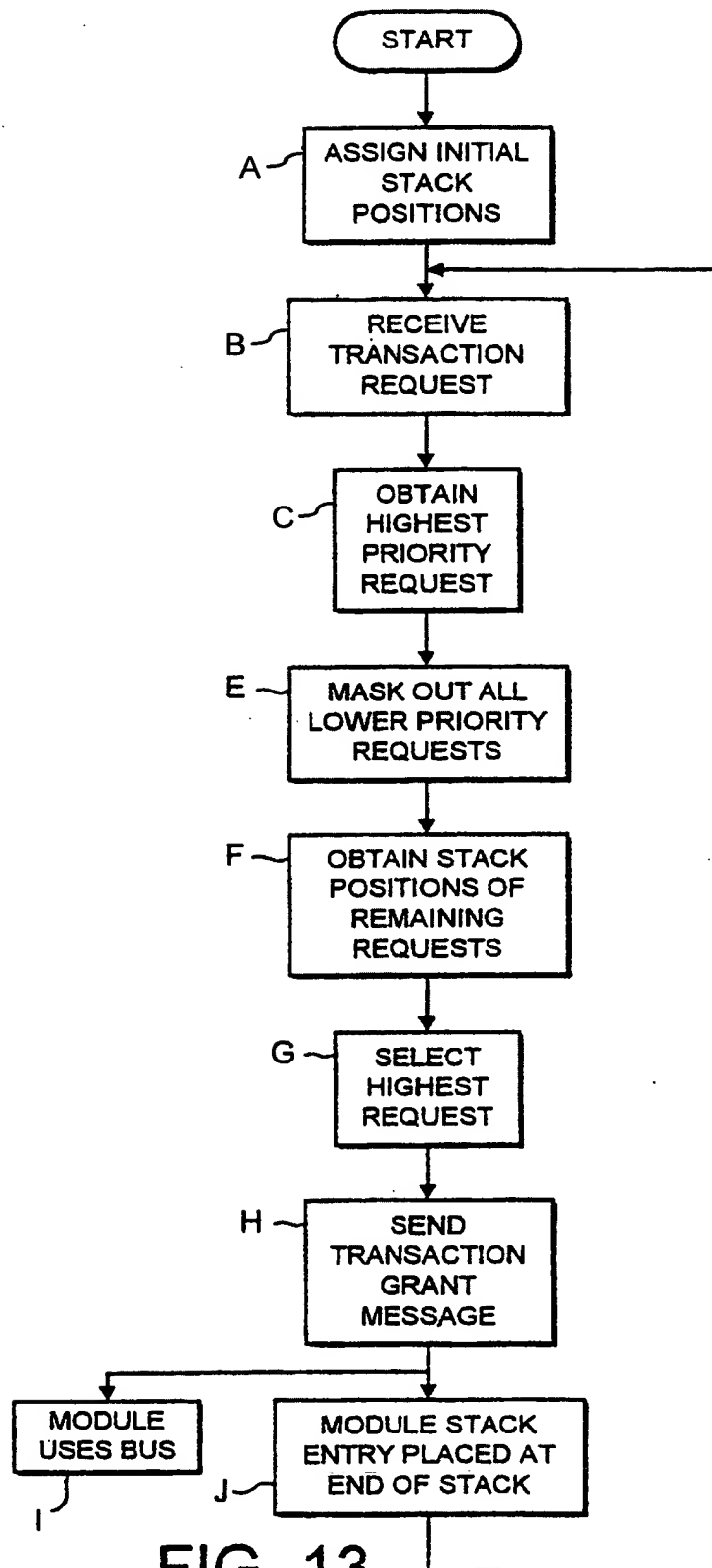


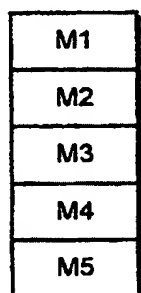
FIG. 13



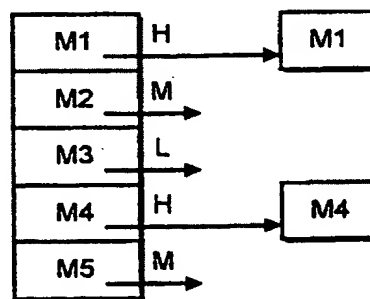
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MODULE	PRIORITY
M1	H
M2	M
M3	L
M4	H
M5	M

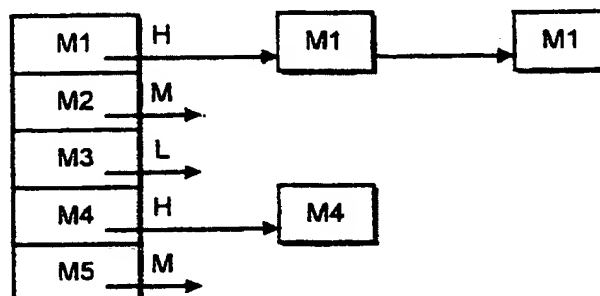
**FIG. 14**



**FIG. 15**



**FIG. 16**



**FIG. 17**

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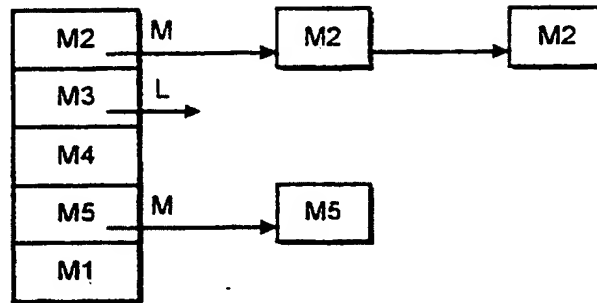
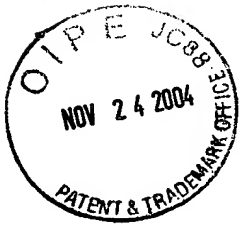


FIG. 18

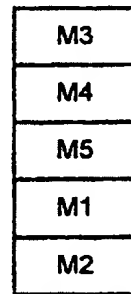


FIG. 19

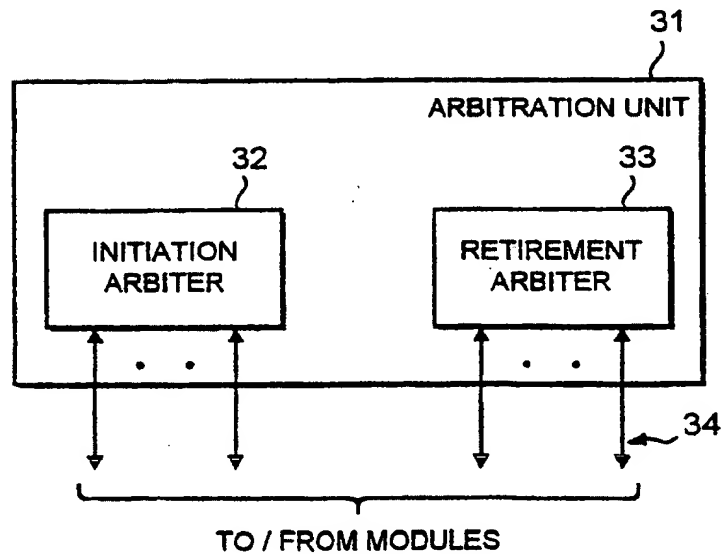


FIG. 20

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T	R1	W1	R2	W2	R3	W3	....	
W		W1A	W1B	W2A	W2B	W3A	W3B	....
R				R1A	R1B			
TIME	t	t	t	t	t	t	t	

FIG. 21

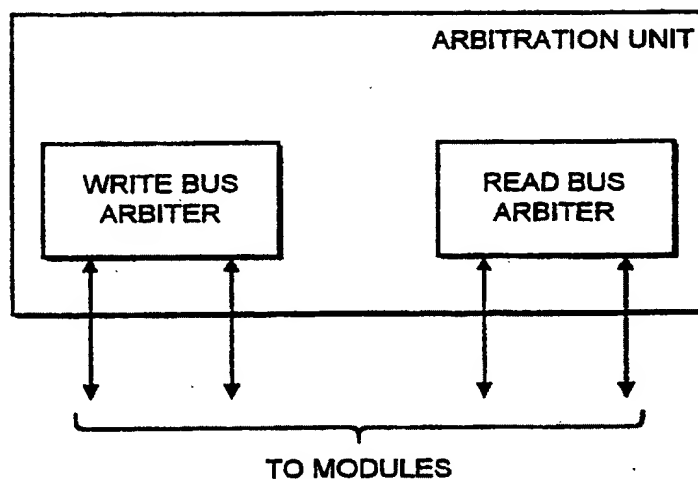


FIG. 22

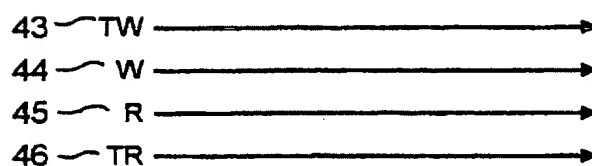


FIG. 23

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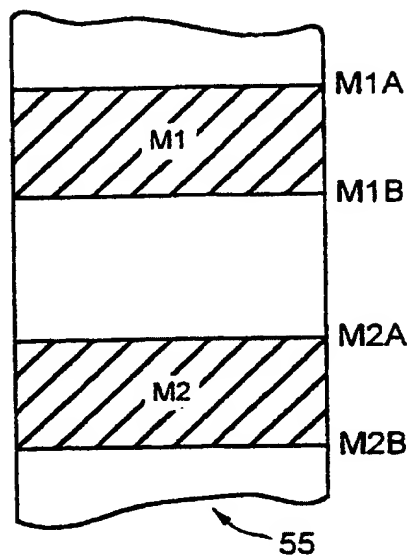


FIG. 26

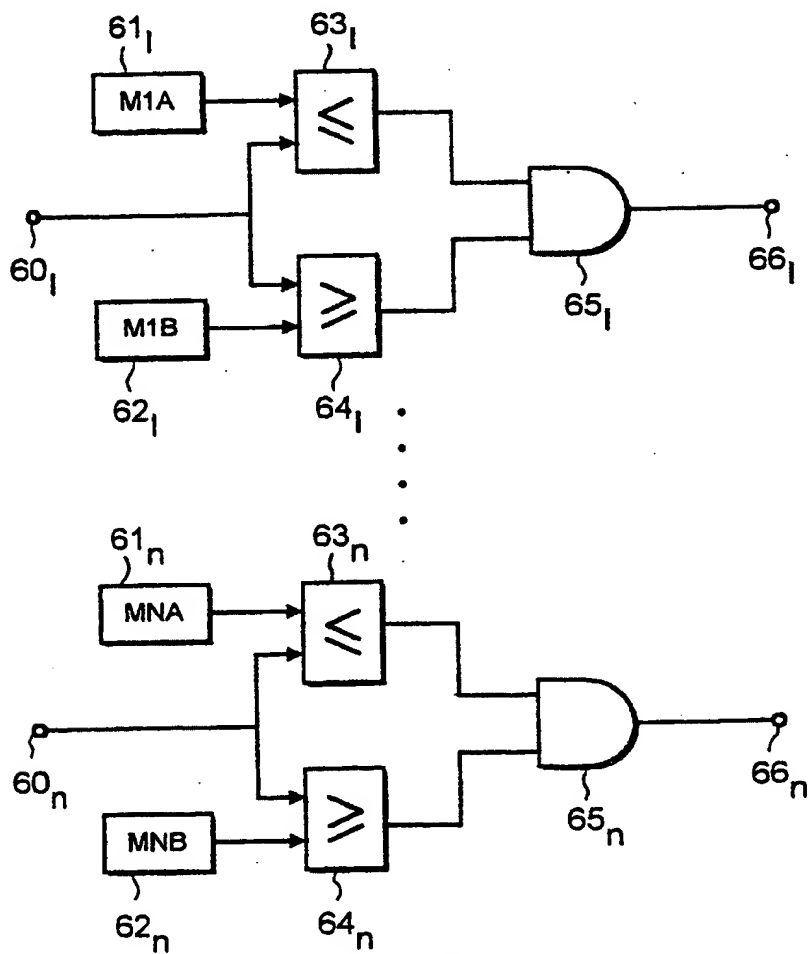
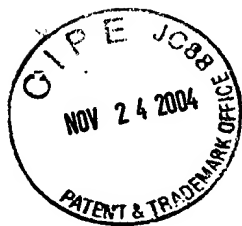
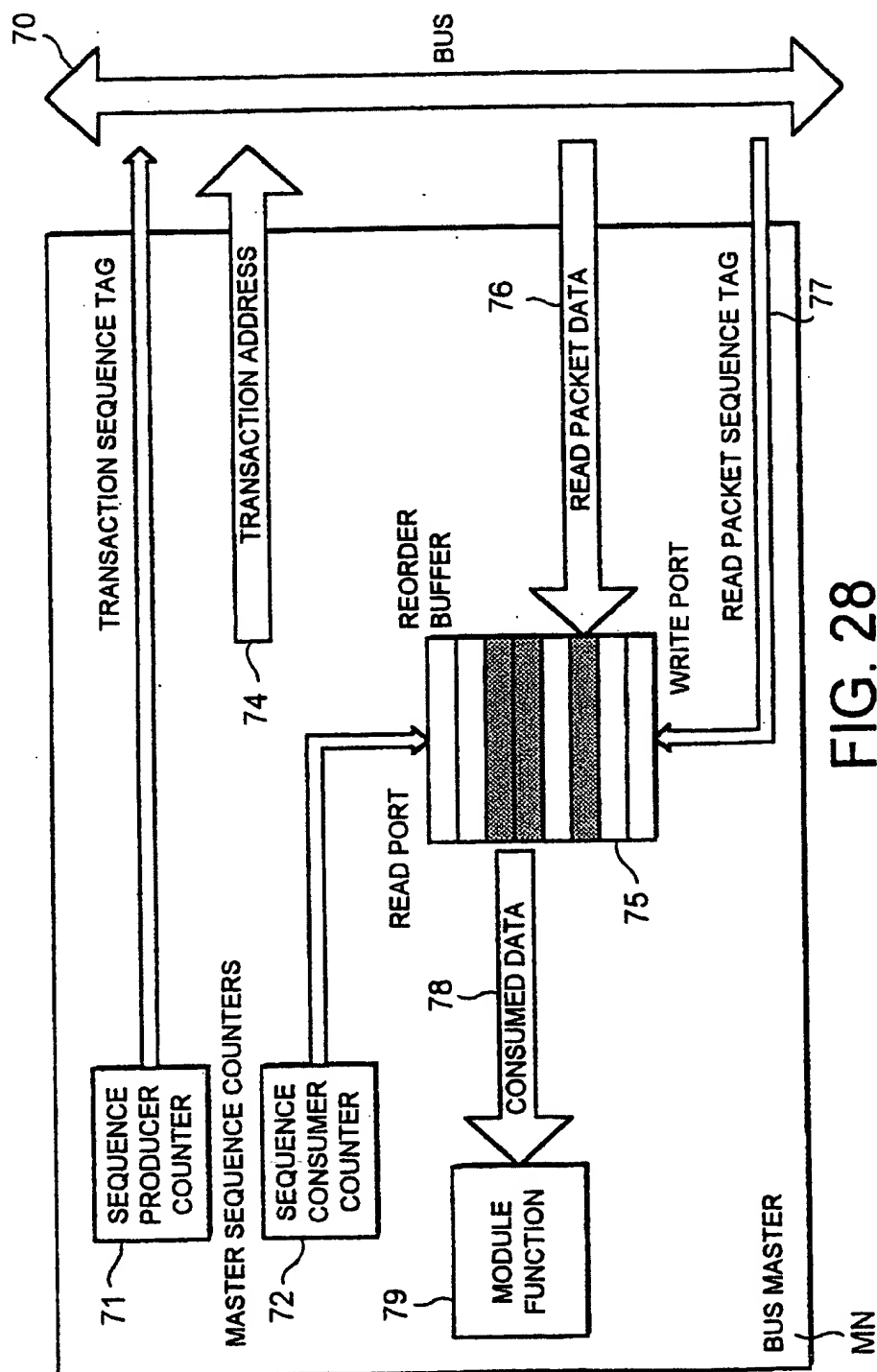
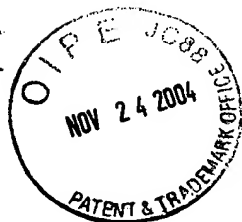


FIG. 27





**FIG. 28**

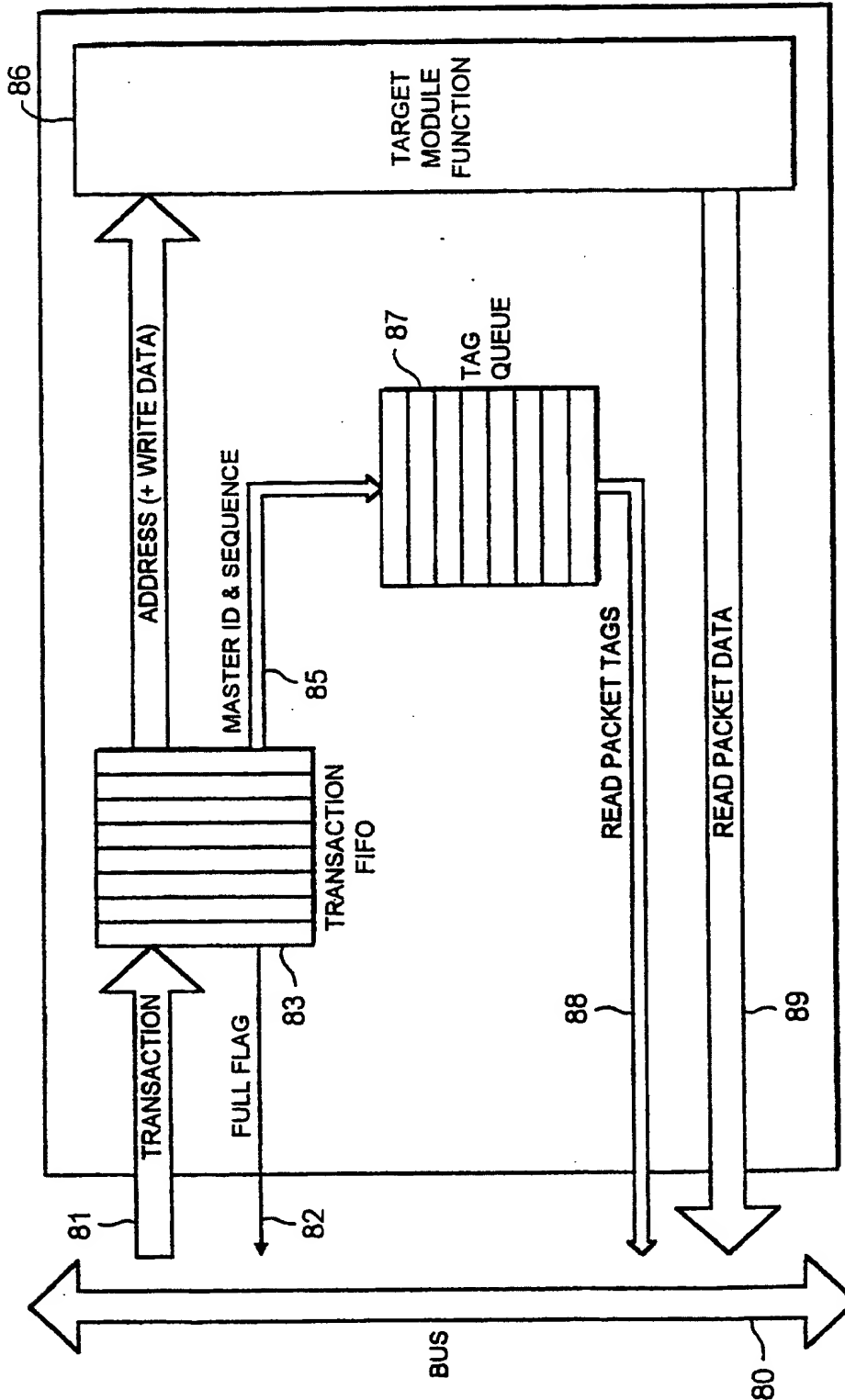
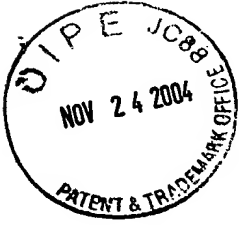


FIG. 29